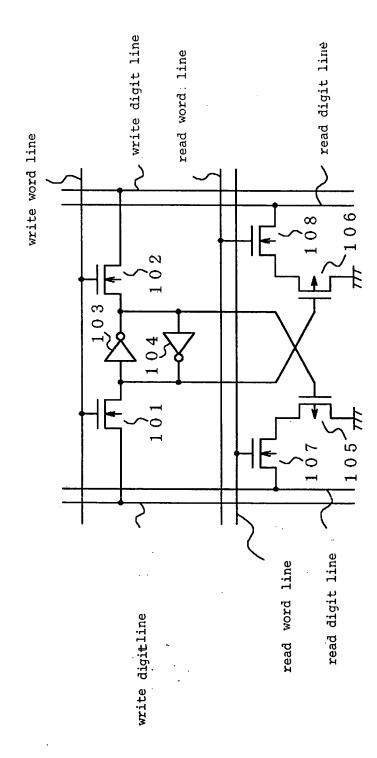
"Data Read Circuit in a Semiconductor Device Featuring Reduced Chip Area and Increased Data Transfer Rate"

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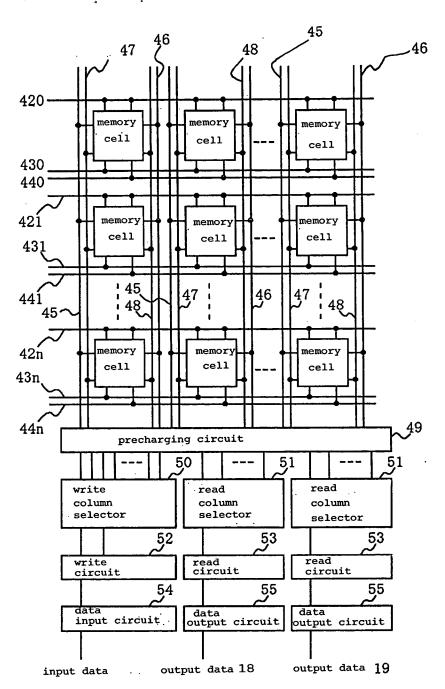
Sheets _____ of 15

Fig. 1 (Prior Art)



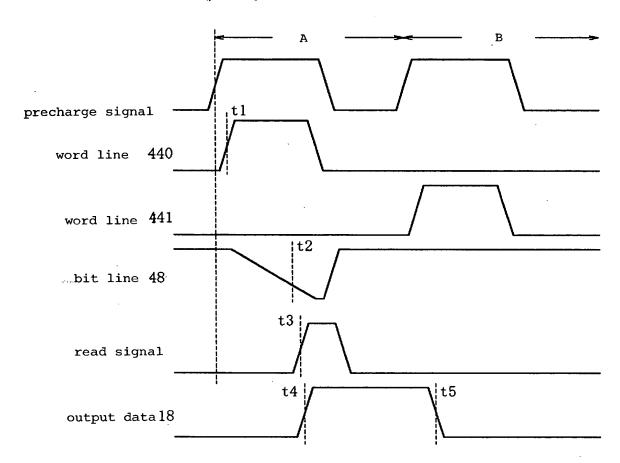
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Fig. 2 (Prior Art)



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Fig. 3 (Prior Art)



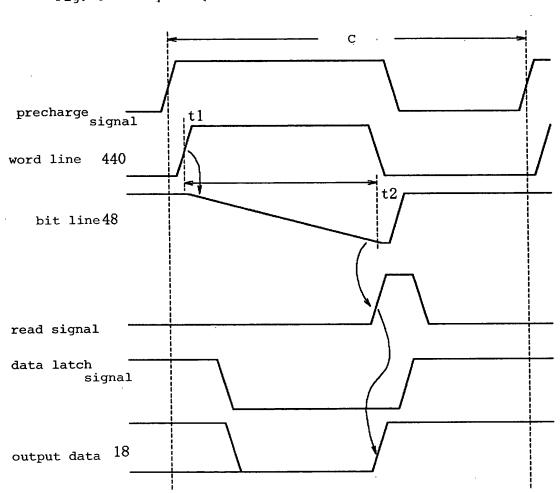
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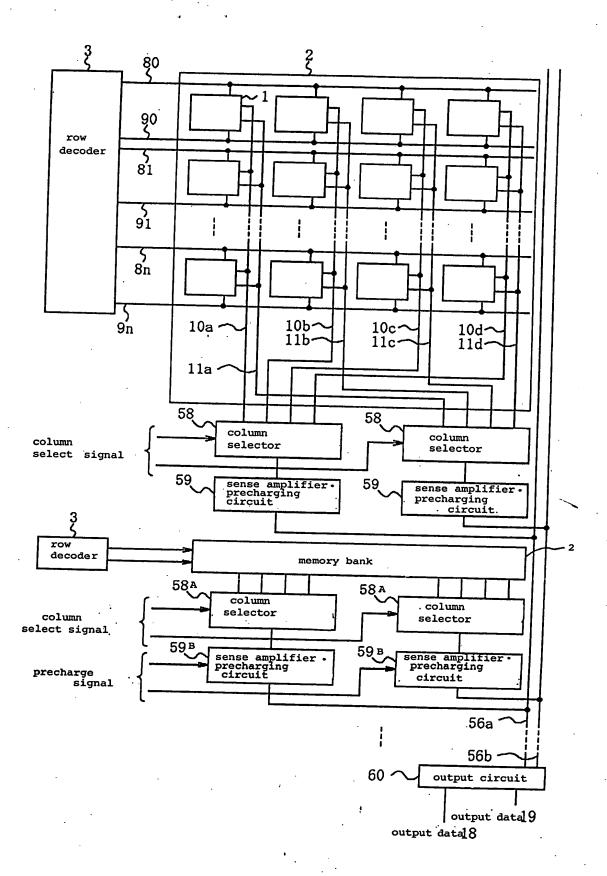
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Fig. 5 (Prior Art)



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Fig. 6 (PrioraArt)

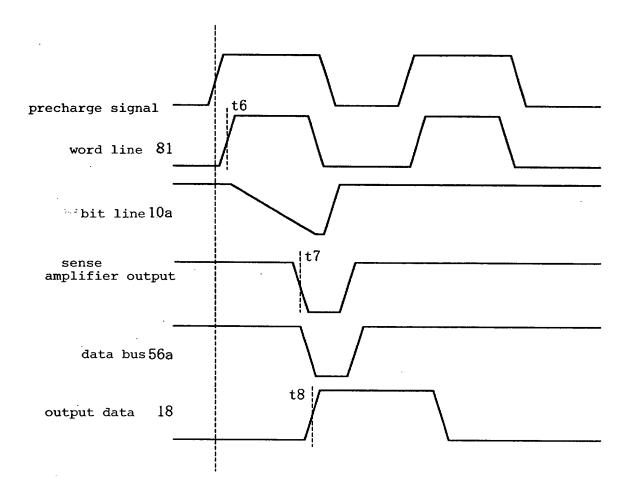
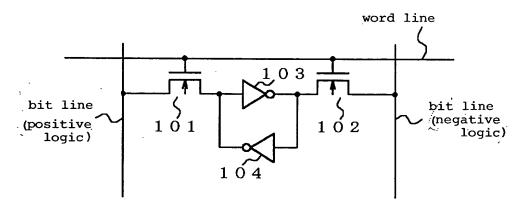
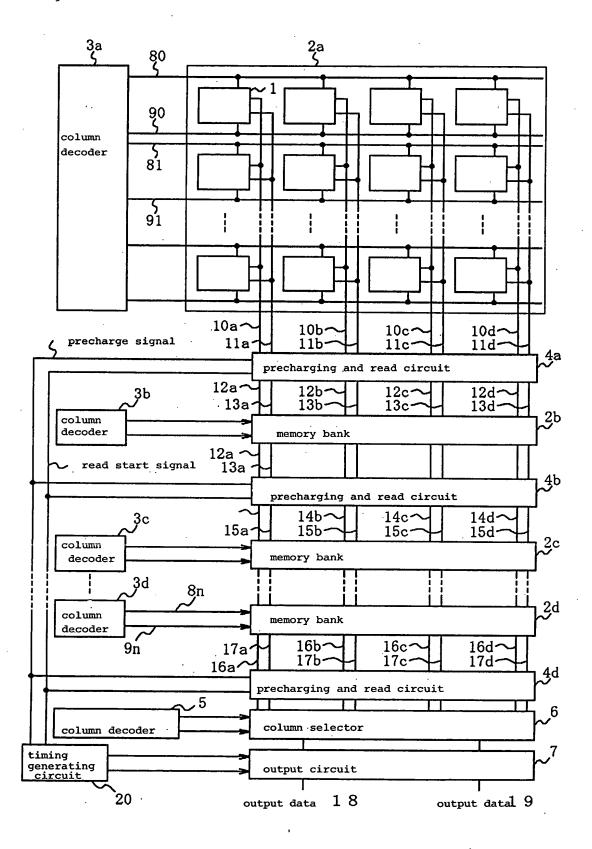


Fig. 7 (Prior Art)



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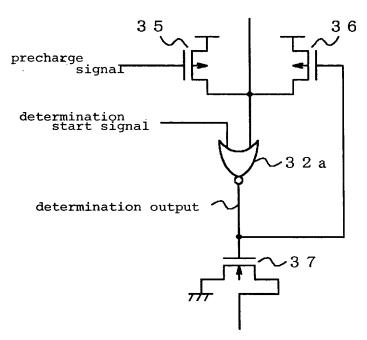
Fig. 8



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Fig. 9

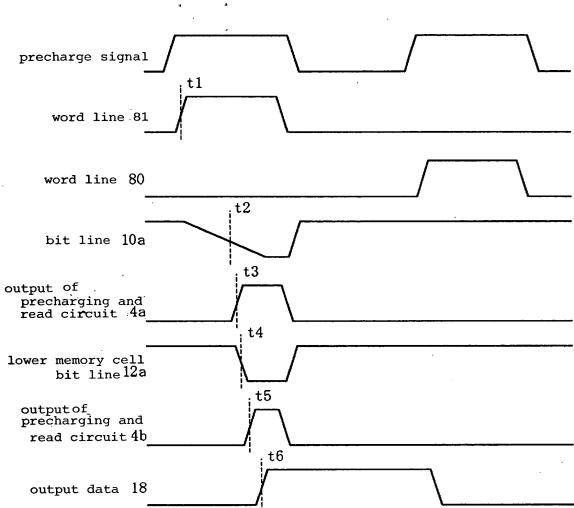
upper block data line



lower block data line

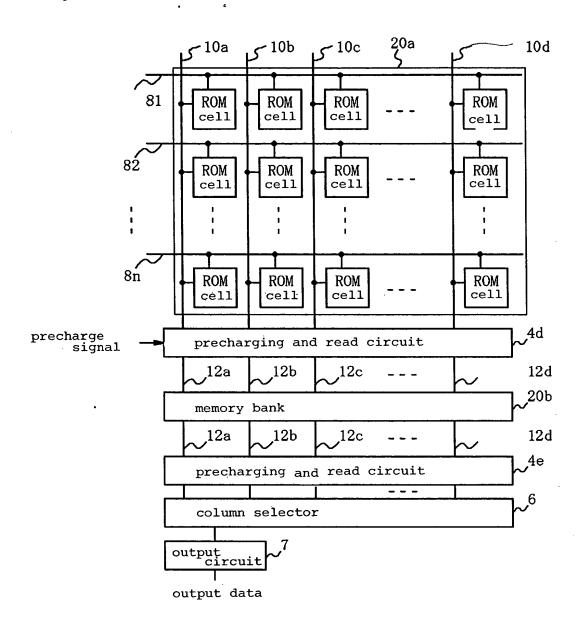
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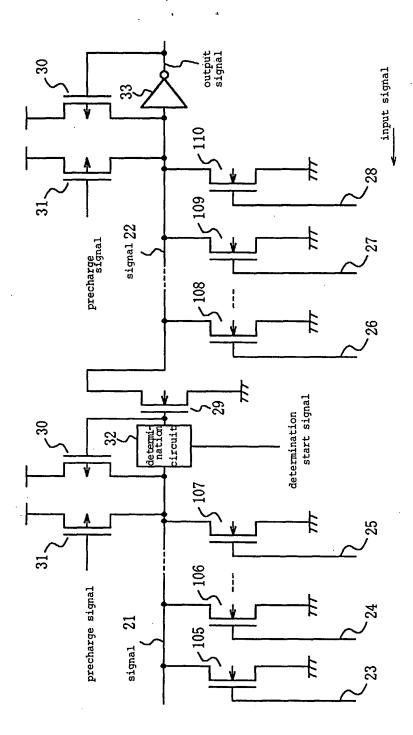
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Fig. 11



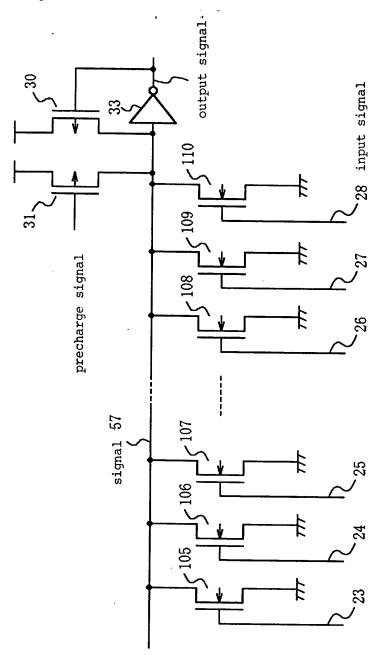
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Fig. 12



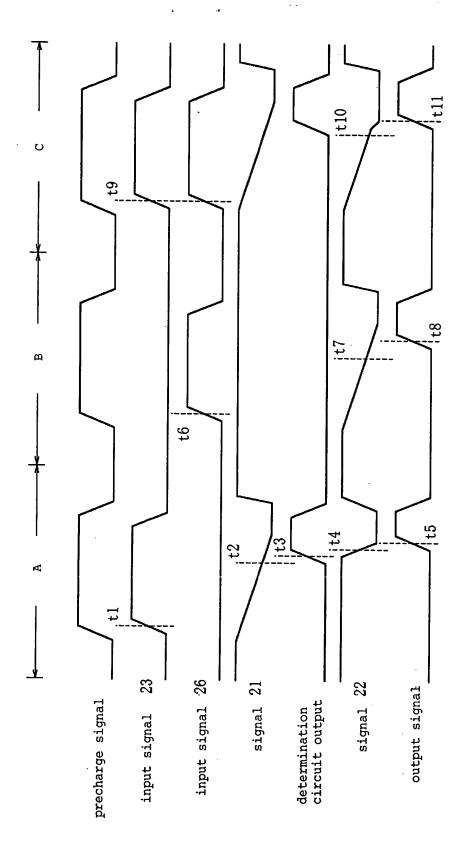
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Fig. 13



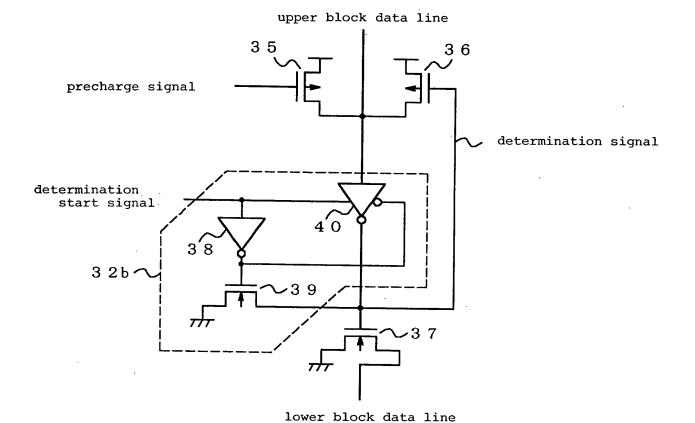
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Fig. 14



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Fig. 15



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Fig. 16

precharge signal

precharge signal

determination start signal

3 5

determination signal

3 2 c

3 7

lower block data signal